ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor memory device has a memory core circuit including a cell array in which electrically rewritable and non-volatile memory cells are arranged therein, decoders configured to select the memory cells, and sense amplifiers configured to perform data read and write of the cell array, and a peripheral circuit including a memory controller configured to control data read and write in communication with the memory core circuit, wherein the memory controller has: an oscillator configured to generate an internal clock signal; a timing control circuit configured to timing control timings of data read and write of the cell array as synchronous with the internal clock signal; and a merge clock generation circuit configured to generate based on an external timing signal and the internal clock signal a merge clock signal serving for timing controlling a circuit portion in the peripheral circuit, the merge clock signal being defined as having a first signal period in which the external timing signal serves as a clock source and a second signal period without overlapping the first signal period, in which the internal clock signal serves as a clock source.